

Notice of Allowability

Application No.

09/638,268

Examiner

Kandasamy Thangavelu

Applicant(s)

BRYAN ET AL.

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to January 14, 2005.
2. ☒ The allowed claim(s) is/are 1,3-5,7-12,15 and 17-21.
3. ☒ The drawings filed on 14 January 2005 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____

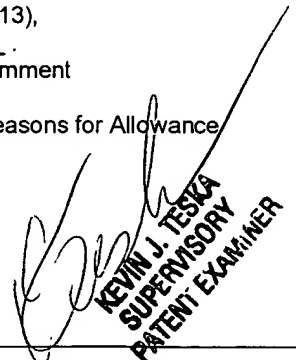
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____


KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated January 14, 2005. Claims 1-21 of the application are pending.

Drawings

2. The drawings submitted on January 14, 2005 are accepted.

Examiner's Amendment

3. Authorization for this examiner's amendment was given in a telephone conversation by Mr. George Pettit on April 8, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

4. In the Claims:

In Claim 1, Lines 1-5, "A method comprising:

Art Unit: 2123

providing a design-under-test (DUT) configuration file comprising a specification of bus transaction types and parameters corresponding to said DUT; and

processing said configuration file to generate a test case comprising bus transactions for verification of said DUT”

has been changed to

-- A method for generating test cases for verification of a device under test (DUT) comprising:

providing a device-under-test (DUT) configuration file comprising a specification of bus transaction types and parameters corresponding to said DUT;

providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case;

evaluating said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases; and

processing said configuration file to generate said test cases comprising bus transactions for verification of said DUT--.

In Claim 2:

Delete claim 2.

In Claim 5, Lines 1-4, “A method comprising:

describing a DUT in a configuration file using a condensed syntax;

Art Unit: 2123

generating a test case for verification of said DUT by converting said condensed syntax into an enumeration of possible parameter combinations for bus transactions of said DUT”

has been changed to

-- A method for generating test cases for verification of a device under test (DUT) comprising:

describing said DUT in a configuration file comprising a specification of bus transaction types and parameters using a condensed syntax;

providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case;

applying said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases; and

generating test cases for verification of said DUT by converting said condensed syntax into an enumeration of possible parameter combinations for bus transactions of said DUT--.

In Claim 6:

Delete claim 6.

In Claim 12, Lines 1-5, “A computer-usable medium storing computer-executable instructions, said instructions when executed implementing a process comprising:

evaluating a syntax of a DUT configuration file including statements defining transaction types and parameters corresponding to said DUT; and

generating bus functional language statements from said syntax”

Art Unit: 2123

has been changed to

-- A computer-usable medium storing computer-executable instructions, said instructions when executed implementing a process for generating test cases for verification of a device under test (DUT) comprising:

providing a device-under-test (DUT) configuration file comprising a specification of bus transaction types and parameters corresponding to said DUT;

providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case;

evaluating a syntax of a DUT configuration file including statements defining bus transaction types and parameters corresponding to said DUT;

testing a parameter combination generated from said configuration file against said rules;

generating bus functional language statements from said syntax; and

outputting said parameter combination in said bus functional language statement when said parameter combination is not excluded by said rules--.

In Claim 13:

Delete claim 13.

In Claim 14:

Delete claim 14.

In Claim 15, Lines 1-7, "A system comprising:

Art Unit: 2123

a memory including computer-executable instructions;
a processor coupled to said memory for executing said instructions; and
a configuration file for a DUT including bus transaction types and parameters
corresponding to said DUT;
wherein said instructions process said configuration file to generate bus transactions for
verification of said DUT”

has been changed to
-- A system for generating test cases for verification of a device under test (DUT)
comprising:

a memory including computer-executable instructions;
a processor coupled to said memory for executing said instructions; and
a configuration file for said DUT including bus transaction types and parameters
corresponding to said DUT;
wherein said configuration file includes rules for including or excluding selected bus
transactions from being generated;
wherein said instructions process said configuration file to generate bus transactions for
verification of said DUT; and
wherein said instructions apply said rules in said configuration file to include or exclude
selected ones of said bus transactions from said test cases--.

In Claim 16:

Delete claim 16.

In Claim 17, Lines 1-4, "A method for generating a test case for a buss interface comprising:

preparing specifications of parameter combinations corresponding to buss transactions of a device under test"

has been changed to

-- A method for generating test cases for verification of a bus interface comprising:

preparing specifications of parameter combinations corresponding to bus transactions of a device under test--.

Reasons for Allowance

5. Claims 1, 3-5, 7-12, 15, 17-21 of the application are allowed over prior art of record.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) simulating the operations of the components of a computer using bus function models; an automated method of generating the simulation code by receiving from the user the addresses for data transfer; the method generates a collection of data transfer instructions with the specified data transfer addresses; the simulation model includes a software implemented interface to a model of the device under test; the method generates simulation model data output

Art Unit: 2123

instructions and data input instructions using the addresses specified; the minimum and maximum number of bytes to be transferred is specified as bus transaction constraint; the bus function model and the DUT operate to simulate data exchange between components of the operating computer system (**Meyer et al.**, U.S. Patent 6,571,204);

(2) an automated test generator for testing computer programs; the user interface of a program is described as a network of choices; the testing program generates the test cases consisting of random data and random series of actions by randomly traversing the network of choices; coverage of combinations of actions superior to manual design of tests is achieved; the generated tests are in the form of test scripts of the testing tool; the programming statements invoke one or more functions of the application program being tested; the test generator uses the application specific information used in the configuration and description files; the description file contains the interface of the application program (**Mongan**, U.S. Patent 6,378,088); and

(3) a system for generating an instruction/data stream used to verify a hardware implementation of an IC design with respect to higher level implementation; the instructions generated thoroughly investigate the boundary conditions, interrupts and exceptions of interest to the particular hardware implementation of the IC; the method receives a plurality of templates, each of which describes the behavior of the IC design on receipt of the instruction; then the method receives a plurality of register models, each of which describes the behavior of registers within the IC; the method then receives a plurality of exception events, each corresponding to potentially problematic operation of the hardware; the method processes the plurality of templates, the register models and exception events to produce the instruction/data stream; the

Art Unit: 2123

instructions when executed by the hardware, verify the results generated by the hardware against the expected results (Shrote, U.S. Patent 5,774,358).

6.1 Applicants' first set of claims consists of Claims 1 and 3-4.

Independent Claim 1 is directed to a method for generating test cases for verification of a device under test (DUT). The claim identifies the uniquely distinct features of:

"providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case;" and

"evaluating said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases".

Because the closest prior art fails to teach or fairly suggest providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case; and evaluating said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases, as claimed by the Applicants, Claims 1 and 3-4 are deemed novel and allowable.

6.2 Applicants' second set of claims consists of Claims 5 and 7-11.

Independent Claim 5 is directed to a method for generating test cases for verification of a device under test (DUT). The claim identifies the uniquely distinct features of:

"providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case;" and

“applying said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases”.

Because the closest prior art fails to teach or fairly suggest providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case; and applying said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases, as claimed by the Applicants, Claims 5 and 7-11 are deemed novel and allowable.

6.3 Applicants' third set of claims consists of Claim 12.

Independent Claim 12 is directed to a computer-usable medium storing computer-executable instructions, said instructions when executed implementing a process for generating test cases for verification of a device under test (DUT). The claim identifies the uniquely distinct features of:

“providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case,”

“testing a parameter combination generated from said configuration file against said rules,” and

“outputting said parameter combination in said bus functional language statement when said parameter combination is not excluded by said rules”.

Because the closest prior art fails to teach or fairly suggest providing rules in said configuration file to include or exclude selected ones of bus transactions from a test case; testing a parameter combination generated from said configuration file against said rules; and outputting said parameter combination in said bus functional language statement when said parameter combination is not excluded by said rules, as claimed by the Applicants, Claim 12 is deemed novel and allowable.

6.4 Applicants' fourth set of claims consists of Claim 15.

Independent Claim 15 is directed to a system for generating test cases for verification of a device under test (DUT). The claim identifies the uniquely distinct features of:

“wherein said configuration file includes rules for including or excluding selected bus transactions from being generated;” and

wherein said instructions apply said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases”.

Because the closest prior art fails to teach or fairly suggest wherein said configuration file includes rules for including or excluding selected bus transactions from being generated; and wherein said instructions apply said rules in said configuration file to include or exclude selected ones of said bus transactions from said test cases, as claimed by the Applicants, Claim 15 is deemed novel and allowable.

6.5 Applicants' fifth set of claims consists of Claims 17-21.

Independent Claim 17 is directed to method for generating test cases for verification of a bus interface. The claim identifies the uniquely distinct features of:

“forming a configuration file of said parameter combinations in a condensed syntax including commands and rules to select various parameter combinations to be included in or excluded from the test case;” and

“generating from said configuration file all bus transactions defined by said rules comprising said test case;”.

Because the closest prior art fails to teach or fairly suggest forming a configuration file of said parameter combinations in a condensed syntax including commands and rules to select various parameter combinations to be included in or excluded from the test case; and generating from said configuration file all bus transactions defined by said rules comprising said test case, as claimed by the Applicants, Claims 17-21 are deemed novel and allowable.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

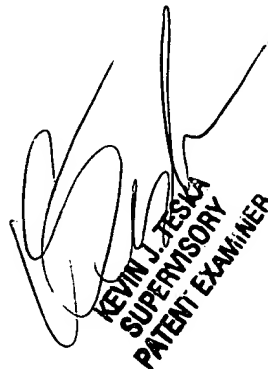
Art Unit: 2123

571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
April 11, 2005



KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER